## aliabit

## **ELECTRONIC INFORMATION DISCLOSURE STATEMENT**

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

JITTER-RESISTIVE DELAY LOCK LOOP CIRCUIT FOR LOCKING DELAYED CLOCK AND METHOD THEREOF

Application Number:  $\sqrt{8}/7/\sqrt{3}/3$ 

Confirmation Number:

First Named Applicant:

Jui-Hsing Tseng

Attorney Docket Number:

MTKP0186USA

Art Unit:

2816

Examiner:

Lina Nguyen

Search string:

(6069507).pn

## **US Patent Documents**

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
LALA	1	6069507	2000-05-30	Shen et al.		327	156

## **Signature**

Examiner Name	Date
La m	02/16/2006